IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

WILLIAM P. STEARNS ET AL.

Serial No. 09/678,318 (TI-25833.1)

Filed October 3, 2000

For: OPTIMIZED CIRCUIT DESIGN LAYOUT FOR HIGH PERFORMANCE BALL GRID ARRAY PACKAGES

Art Unit 2815

Examiner P. Brock, II

Commissioner for Patents
Washington, D. C. 20231

Sir:

AMENDMENT UNDER 37 C.F.R. 1.111

In response to the first Office action dated April 25, 2001, please amend the above identified application as follows:

In the claims:

Amend claim 1 as follows:

1. (Amended) A method of laying out traces for connection of bond pads of a semiconductor chip to a ball grid array disposed on a substrate, [printed wiring board substrate or the like] which comprises the steps of:

(a) providing a substrate having a surface with a plurality of rows and columns of ball pads and having a solder ball secured to each of said ball pads; and